# Deterministic DEM DAC Performance Analysis

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***Abstract*— A rigorous and complete analysis of the Deterministic DEM (DDEM) DAC performance is presented. With this analysis, DDEM DAC's equivalent linearity as ADC static linearity test stimulus source can be precisely predicted. Simulation result is given to validate this theoretical analysis.**

***Key Words*— Deterministic DEM DAC, ADC, built-in self-test, equivalent linearity**

## I. INTRODUCTION

Built-in self-test (BIST) is viewed as the most promising solution to testing today's high-resolution high-speed ADCs, especially those deeply embedded in SoC applications [1]. For the past decade, researchers have gained great improvements in building cost-effective stimulus sources for ADC BIST. [2] However, conventional types of stimulus source, such as linear ramp generators and high performance DACs, cannot meet the requirement of testing today's high performance ADCs, either due to insufficient linearity or high implementation cost.

The deterministic dynamic element matching (DDEM) technique was proposed as a solution to this problem [3]. In this technique, DDEM cyclic switching control is applied on low accuracy/linearity DACs to generate stimulus signals for high resolution ADC static linearity BIST. Figure 1 shows the block diagram of this solution.

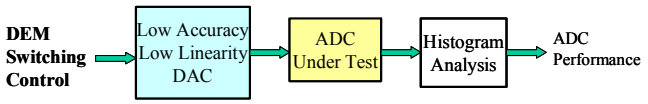


Figure 1. DDEM technique for ADC BIST

The mechanism of the DDEM technique was explained in [4] by examining the output probability distribution function (PDF) based on the analysis of the "averaged" DAC. This analysis answers the question why low resolution/linearity DACs with DDEM control can be used for high resolution ADC static linearity test. In [5], attempt was made to evaluate the performance for a given DDEM DAC quantitatively. A formula was given to predict the equivalent linearity of a DDEM DAC as ADC static linearity test stimulus source. This formula matches the simulation results well when the DAC resolution and DDEM iteration number are low. However, simulation results show that remedies must be made to this formula when the DDEM DAC resolution goes high.

In this paper, rigorous and complete analysis is presented to inspect the performance of DDEM DACs. With both the random element mismatching errors and quantization errors included in this analysis, a new formula is derived to predict the equivalent linearity of a given DDEM DAC. The predicted performance using this formula matches the simulation results well even for modest-high resolution DDEM DAC with large DDEM iteration number.

This paper is organized as following. In Section II, the DDEM method is reviewed, symbols are defined and performance evaluation criterion is established. Rigorous and complete analysis of the DDEM DAC equivalent linearity as ADC static linearity test stimulus source is presented in Section III. Simulation result is given in Section IV to correlate the theoretical result. The work is concluded in Section V.

## II. DDEM DAC AND EVALUATION CRITERION

In this section, the cyclic DDEM switching sequence for a current steering thermometer-coded DAC is reviewed.

A normal $n$-bit thermometer-coded DAC has $2^n$-1 current source elements. In the DDEM DAC, one extra current source element has been added so that an $n$-bit DDEM DAC has a total of $N = 2^n$ current sources. We use $i_j \quad (j = 1,..., N)$ to represent the j-th current source element out of the total $N$ elements.

For a digital word "$k$", the DDEM method deterministically picks the $k$ current sources to be switched on. Multiple outputs are generated for each digital word "$k$" with different deterministically selected current source combinations. The number of outputs per DAC input code is denoted as $p$. $p$ is also termed as the DDEM iteration number. An integer $q$ is defined by the expression $q = N/p$.

Figure 2 illustrates the general idea of the DDEM technique with a 5-bit DDEM DAC as an example. To show the switching sequence, the current sources are arranged conceptually and sequentially around a circle, as seen in Figure 2, to visualize a wrapping effect whereby the $N_{th}$ current source $i_N$ is adjacent to the first current source $i_1$. $p$

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index current elements uniformly spaced around the circle are selected from all the $N$ elements. For each input code $k$, the DDEM DAC generates $p$ output voltage samples with each obtained by consecutively switching on $k$ current sources starting from one of the $p$ index current sources. In Figure 2, $p$=8, and the 1st, 2nd, 5th and 8th output sample out of all the 8 output samples corresponding to DAC code 10 are depicted. The resistor $R_C$ is chosen so that when all of the current sources are on, the voltage output is at the desired maximum.

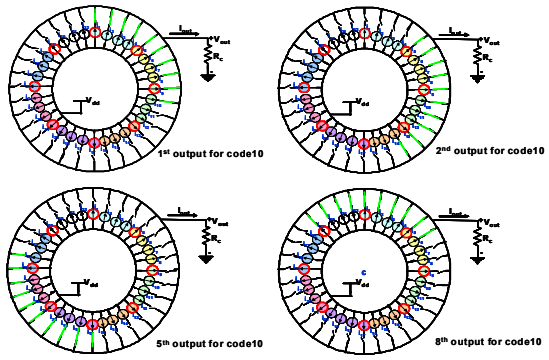


Figure 2. DDEM DAC Example -- 5-bit DAC w/ 3-bit DDEM Control

The aim of a DDEM DAC is to output voltage samples with uniform histogram for histogram-based ADC static linearity test. Assume that the stimulus to the DUT (ADC) has a voltage range [$V_{smin}$, $V_{smax}$] and the ADC input voltage range is [$V_{min}$, $V_{max}$]. The stimulus voltage range should cover the DAC input range. For an arbitrary voltage, $V_t$, let $h(V_t)$ represent the number of stimulus voltage samples that falls into [$V_{smin}$, $V_t$]. The linearity of $h(V_t)$ with respect to $V_t$ will determine ADC test accuracy. [6] Define the error expression $e(V_t)$ as

$$e(V_t) = h(V_t) - h(V_{\min}) - C_h \cdot (V_t - V_{\min}) \qquad (1)$$

in which the constant $C_h$ is the ideal value of $(h(V_t) - h(V_{\min}))/(V_t - V_{\min})$. The DDEM DAC performance will be evaluated by estimating $e(V_t)$.

## III. DDEM DAC Equivalent Linearity

In the following, the ADC test performance using the DDEM DAC as the test stimulus source will be evaluated by deriving $e(V_t)$ as defined in (1), for any voltage, $V_t$, in ADC input range [$V_{min}$, $V_{max}$].

We first expand the number of current sources virtually to $2N$ by letting $i_{N+r} = i_r \ \ (r = 1,...,N)$. Then, virtually, we have $2N$ current sources: $i_1, i_2, ..., i_N, i_{N+1}, ..., i_{2N}$.

Let $V_0[0] = 0$ and $V_0[k] = R_C \cdot \sum_{r=1}^{k} i_r ...(k = 1,...,2N)$, in which $R_C$ is the output resistance of the DDEM DAC. Note that the first half of the sequence is the output voltage sequence of a regular $n$-bit DAC. Let $V_m = V_0[N]$, and $V_m$ is the maximum output of the DDEM DAC. Define $LSB = V_m / N$.

Now, define $INL[k]$ and $DNL[k]$ for the original DAC without DDEM.

$$INL[k] = (V_0[k] - k \cdot LSB)/LSB .....(k = 0,...,2N)$$

$$DNL[k] = (V_0[k] - V_0[k-1] - LSB)/LSB .....(k = 1,...,2N)$$

From this definition, we have:

$$INL[k] = \sum_{r=1}^{k} DNL[r] .....(k = 1,...,2N) \qquad (2)$$

$$\sum_{r=k}^{k+N-1} DNL[r] = 0 .....(k = 1,..., N) \qquad (3)$$

With the DDEM cyclic switching sequence, the DAC outputs $p \cdot N$ output voltage samples. These $p \cdot N$ output voltage samples can further be decomposed into $p$ ramps with $N$ samples in each ramp. The 1st ramp is given by $R_C \cdot \sum_{r=1}^{k} i_r \ \ (k = 1,..., N)$. The d-th ($1 \le d \le p$) ramp is given by $R_C \cdot \sum_{r=1+q(d-1)}^{k+q(d-1)} i_r \ \ (k = 1,..., N)$, or rewritten as

$$\{V^{(d)}[k]\} = \{V_0[k + q(d-1)] - V_0[q(d-1)] : 1 \le k \le N\}.$$

For an arbitrary voltage $V_t$ less than $V_m$, let $h^{(d)}(V_t)$ represent the number of elements less than $V_t$ in $\{V^{(d)}[k]\}$.

$$h^{(d)}(V_t) = \left|\{V^{(d)}[k] : V^{(d)}[k] \le V_t, 1 \le k \le N\}\right|$$

The definition of $h^{(d)}(V_t)$ can be explained using Figure 3.a. In this figure, $N$+1 mark arrows on an axis represent the $d$-th ramp sequence. The relative position of the $k$-th($1 \le k \le N$) arrow on the axis represents the value of $V^{(d)}[k]$. By definition, $V_t$ is located between the [ $h^{(d)}(V_t)$ ]-th sample (arrow) and the [ $h^{(d)}(V_t)+1$ ]-th sample.

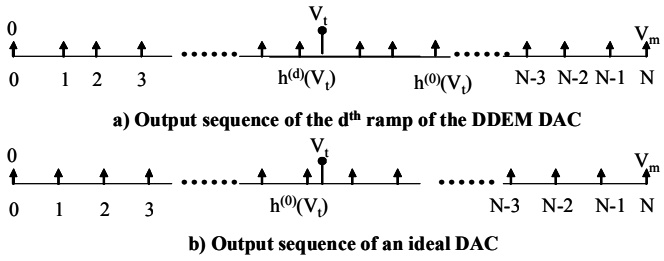


Figure 3. Nonideal and ideal DAC output sequences

Let $h^{(0)}(V_t) = floor(N \cdot V_t / V_m) = |\{k : k \cdot LSB \le V_t, 1 \le k \le N\}|$, in which $0 \le h^{(0)}(V_t) \le N$. $h^{(0)}(V_t)$ is marked on the axis in Figure 3.b with uniformly spaced arrows, corresponding to the output voltages of an ideal DAC. For a non-ideal DAC, $h^{(d)}(V_t)$ deviates from $h^{(0)}(V_t)$, as shown in Figure 3. The

difference between $V_t$ and the [ $h^{(0)}(V_t)$ ]-th sample in the sequence $\{V^{(d)}[k]\}$ reflects the DAC INL at code $h^{(d)}(V_t)$. This voltage difference divided by the DAC LSB can be used to approximate the difference between $h^{(0)}(V_t)$ and $h^{(d)}(V_t)$. Here, the approximation is based on the assumption that the local DNL of the DAC sequence is not large, and this assumption is valid for thermometer-coded DAC design. The approximation error can be viewed as a quantization error and is distributed over the range of $(-0.5, 0.5]$. Denote this error as $\varepsilon^{(d)}$. Thus, we have the following expression for $h^{(d)}(V_t)$:

$$h^{(d)}(V_t) = h^{(0)}(V_t) + \frac{V_t - V^{(d)}\left[h^{(0)}(V_t)\right]}{LSB} + \varepsilon^{(d)} \quad (1 \le d \le p) \quad (4)$$

For every d, if we apply (2), we have:

$$V^{(d)}[h^{(0)}(V_t)] = V_0[h^{(0)}(V_t) + q(d-1)] - V_0[q(d-1)]$$
$$= LSB \cdot \left(INL[h^{(0)}(V_t) + q(d-1)] - INL[q(d-1)] + h^{(0)}(V_t)\right)$$
$$= LSB \cdot \left( \sum_{k=1}^{h^{(0)}(V_t)} DNL[k + q(d-1)] + h^{(0)}(V_t) \right)$$

Substitute this into (4), we have:

$$h^{(d)}(V_t) = \frac{V_t}{LSB} - \sum_{k=1}^{h^{(0)}(V_t)} DNL[k + q(d-1)] + \varepsilon^{(d)} \quad (1 \le d \le p) \quad (5)$$

Now calculate $h(V_t)$ and $e(V_t)$ as defined in Section II. $h(V_t)$ denotes the total number of DDEM DAC voltage samples that are less than $V_t$.

$$h(V_t) = \sum_{d=1}^{p} h^{(d)}(V_t)$$
$$= p\frac{V_t}{LSB} - \sum_{d=1}^{p} \sum_{k=1}^{h^{(0)}(V_t)} DNL[k + q(d-1)] + \sum_{d=1}^{p} \varepsilon^{(d)}$$

Let $h^{(0)}(V_t) = q \cdot t + m \ (0 < m \le q, 0 \le t < p, t \,\&\, m \in Z)$. Applying (3) leads to:

$$h(V_t) = p\frac{V_t}{LSB} - \sum_{d=1}^{p} \sum_{k=1}^{m} DNL[k + q(d-1)] + \sum_{d=1}^{p} \varepsilon^{(d)} \quad (6)$$

$C_h$ defined in (1) is given by $C_h = \frac{pN}{V_m}$ for this DDEM DAC. Then by definition,

$$e(V_t) = p\frac{V_t}{LSB} - \sum_{d=1}^{p} \sum_{k=1}^{m} DNL[k + q(d-1)] - \frac{pN}{V_m} \cdot V_t + \sum_{d=1}^{p} \varepsilon^{(d)}$$

$\frac{pN}{V_m} \cdot V_t$ is exactly $p\frac{V_t}{LSB}$ by definition. If we change the order of DNL[k] summation, we have:

$$e(V_t) = -\sum_{k=1}^{m} \sum_{d=1}^{p} DNL[k + q(d-1)] + \sum_{d=1}^{p} \varepsilon^{(d)} \quad (7)$$

$e(V_t)$ is composed of two items. The first item is a summation of DAC *DNL*[*k*]'s, and can be treated as the INL of an *n*-bit DAC. The second item is caused by the quantization effect. We can approximately assume that $\{\varepsilon^{(d)}\}$ have a standard deviation of $1/\sqrt{12}$, since the quantization error is normally treated to have a uniform distribution over the range of $(-0.5, 0.5]$ with the standard deviation equal to $1/\sqrt{12}$. Hence, the standard deviation of the second item is given by $p/\sqrt{12}$ if $\varepsilon^{(d)}$'s are independent.

When $p$ is small, the first item in (7) dominates. We can ignore the quantization error item and approximate $e(V_t)$ to:

$$e(V_t) \approx -\sum_{k=1}^{m} \sum_{d=1}^{p} DNL[k + q(d-1)]$$

Since the full range of $h(V_t)$ is $p \cdot N$, the percentage error in the DDEM DAC output voltage sample's distribution is bounded by INL/$p \cdot N$. The DDEM DAC has an equivalent accuracy of $n_{eq}$ bits, where $n_{eq}$ is given by:

$$n_{eq} \approx \log_2\left(pN/(INL/0.5)\right) \approx n + 1 + \log_2 p - \log_2 INL$$

The DAC effective number of bits (ENOB) is defined by $n - \log_2(INL/0.5)$, giving:

$$n_{eq} \approx ENOB_{DAC} + \log_2 p$$

This means that $n_{eq}$ increases by 1 bit every time $p$ doubles when $p$ is small. However, as $p$ becomes very large, the second item can become larger than the first item. When $p$ is adequately large, the second item $\sum_{d=1}^{p} \varepsilon^{(d)}$ dominates. Under the situation that $\varepsilon^{(d)}$'s are independent, the standard deviation of $\sum_{d=1}^{p} \varepsilon^{(d)}$ is inversely proportional to $\sqrt{p}$ when normalized to $p \cdot N$. This means that, when $p$ is large, $n_{eq}$ increases by 0.5 bit every time $p$ doubles. A trip point $p_T$ happens when $\frac{\sqrt{p}}{\sqrt{12}}$ is comparable to the INL of the original DAC. For this trip point $n_{eq}$ incremental speed changes from 1 bit to 0.5 bit for doubling $p$. When $p$ is equal to $p_T$, $\sum_{d=1}^{p} \varepsilon^{(d)}$ is comparable to the first item in (7) in magnitude, and the summation of these two items gives $n_{eq} \approx ENOB_{DAC} + \log_2 p_T - 1$ in the worst case that the magnitudes of these two items are added.

In summary, we have the following formula for the equivalent linearity of a DDEM DAC:

$$n_{eq} \approx \begin{cases} ENOB_{DAC} + \log_2 p & p < p_T \\ ENOB_{DAC} + \log_2 p_T - 1 & p = p_T \\ ENOB_{DAC} + \log_2 p_T - 1 + 0.5\log_2(p/p_T) & p > p_T \end{cases} \quad (8)$$

in which $p_T$ is given by solving $\frac{\sqrt{p_T}}{\sqrt{12}} \approx INL_{DAC}$.

Equation (8) is obtained based on the assumption that $\varepsilon^{(d)}$'s are independent. The correlation among $\varepsilon^{(d)}$'s can affect in two aspects. First, $p_T$ will be smaller than what is expected. Secondly, when $p$ is larger than $p_T$, we have:

$n_{eq} \approx ENOB_{DAC} + \log_2 p_T - 1 + \alpha \log_2(p/p_T)$

in which $\alpha$ is less than 0.5.

## IV. Simulation Correlation

To validation the analysis presented in Section III, simulation was done to compare the 12-bit DDEM DAC performance with different DDEM iteration numbers $p$, and the equivalent linearity was quantized to draw a curve. In the simulation, the DAC has 4096 randomly generalized current elements with the same normal distribution, and the normalized standard deviation is set to be 6%. The DDEM DAC is used to test a simulated 14-bit ADC. Although the simulation result of only one DAC-ADC pair is shown here, the result is repeatable for all the random generalized DAC-ADC pairs in simulation.

The original DAC's INL is about 4 LSB. By definition, this DAC's ENOB is about 9 bits. The DDEM DAC's output samples are used as the stimulus for the 14-bit ADC linearity test. The ADC INL[$k$] test errors (difference between estimated INL[$k$] and true INL[$k$]) are compared under different DDEM iteration number $p$ ranging from 8 to 1024. Figure 4 shows ADC INL[$k$] test error curves when p is 8, 32, 128, and 512, respectively. It is clear that test errors decrease when $p$ increases.

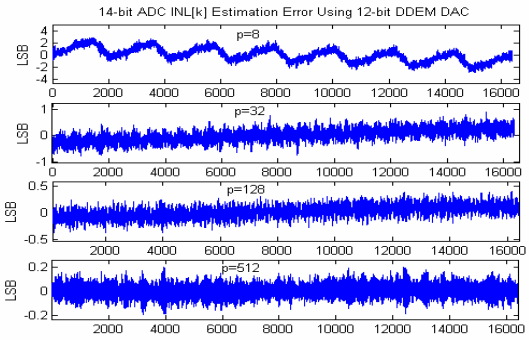


Figure 4. ADC test errors under different p

Under each $p$, the DDEM DAC equivalent linearity is calculated from the above simulation results. Basically, if we use a 14-bit ideal DAC to test a 14-bit ADC, the maximum INL[$k$] test error (absolute value) will be about 1 LSB. Based on this, if the test error is $\varepsilon$ LSB, we can claim that the test stimulus source has an equivalent linearity of $14 - \log_2 \varepsilon$ bits. With this definition, the 12-bit DDEM DAC equivalent linearity under different $p$ is calculated and shown in Figure 5. Theoretical prediction using (8) is also drawn in Figure 5.

Note solving $\frac{\sqrt{p_T}}{\sqrt{12}} \approx INL_{DAC}$ gives $p_T \approx 192$. Since $log_2 p$ can only be an integer, we can take $p_T = 128$. It can be seen that the theoretical prediction according to (8) matches the simulation result quite well. The small theoretical prediction error mainly comes from the approximation in (8).

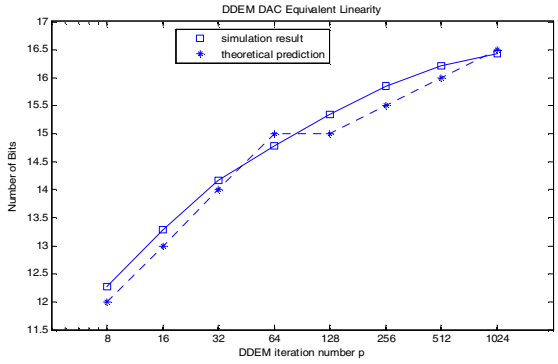


Figure 5 Simulated result and theoretical predction of DDEM DAC $n_{eq}$

## V. Conclusion

The performance of a DDEM DAC as the ADC static linearity test stimulus source has been analyzed rigorously in this paper. A formula is given to predict the DDEM DAC equivalent linearity quantitatively. The theoretical prediction matches the simulation results well. This analytical result can be used to determine the DAC number of bits, element size, and number of DDEM control bits for cost-effective DDEM DAC implementation.

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